REMARKS

Applicant would like to thank the Examiner for the careful consideration given the present application. The application has been carefully reviewed in light of the Office action, and amended as necessary to more clearly and particularly describe the subject matter which applicant regards as the invention.

Initially, claim 8 is objected to for depending from a rejected claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim. Claim 8 has been amended into independent form, and is now in a condition indicated by the Examiner as allowable.

Claims 3, 5, 6, 11 – 14, and 16 were rejected under 35 U.S.C. 102(e) as being anticipated by U.S. Patent No. 6,911,728 to Ishikawa et al. (hereinafter, "Ishikawa"). The rejections are traversed for the following reasons.

The invention defined in claim 3 is directed to a semiconductor device. The device includes a semiconductor element, a heat sink, and a laminar plate including an intermediate layer for moderating thermal stress provided between the semiconductor element and the heat sink. The laminar plate includes first, second, and third metal plates, with an intermediate layer between the first and second plates, and an insulating member between the second and third plates, each of the members being bonded to one another. Further, one side of the first metal plate is bonded to the semiconductor element. Additionally, claim 3 has been amended to define that the semiconductor element and the heat sink have different coefficients of thermal expansion, and that the intermediate layer absorbs and moderates the thermal stress caused by the different coefficients of thermal expansion.

Ishikawa teaches an electronic component having multiple layers. Specifically, in order, the electronic component includes an IC chip (108), an Ni layer (128), a solder layer (124), a second Ni layer (126), an upper electrode layer (116), an insulating layer (114), a lower electrode layer (112), a third Ni layer (122), a solder layer (120), a fourth Ni layer (110), and a heat sink (102).

While Ishikawa teaches a layered component, Ishikawa fails to teach the specific laminar plate constitution recited in claim 3. Initially, claim 3 recites first, second, and third metal plates. The first metal plate of claim 3 has "one side bonded to the semiconductor element and an opposite side bonded to a first side of the intermediate layer". With reference to the Ishikawa device, the IC chip (108) is disposed above an Ni layer (128), which is above a solder layer (124), which is above a second Ni layer (126), which is directly above the layer cited as teaching the second metal plate of claim 3 (the upper electrode 116). Accordingly, to anticipate claim 3, one of the Ni layer (128), the solder layer (124), and the second Ni layer (126) must teach the first metal plate, and another must teach the intermediate layer, with the member teaching the first metal plate being bonded to the IC chip (108) and the intermediate layer, and the intermediate layer being bonded to the upper electrode (116).

In this regard, the Ishikawa device fails to teach a first metal plate and intermediate layer as recited in claim 3. In the rejection, the Examiner refers to the second Ni layer (126) as teaching both the first metal plate and the intermediate layer of claim 3. Claim 3 specifically recites that the first metal plate and the intermediate layer are separate layers that are bonded to one another. A single Ni plated layer cannot be cited for teaching two layers that are bonded to one another.

Thus, if the Ni layer (126) is considered to teach the first metal plate, then Ishikawa fails to teach an intermediate layer disposed between the first metal plate and the second metal plate.

Further, the Ni layer (126) of Ishikawa cannot be cited as teaching the intermediate layer of claim 3. Claim 3 requires that the intermediate layer is "for absorbing and moderating thermal stress". It is submitted that a Ni layer does not provide this function, and therefore cannot be cited for teaching the intermediate layer of claim 3. The Ni plated layers merely improve the wettability of the layers to improve bonding. Further, no other layer disposed between the upper electrode (116) and the IC chip (108) of Ishikawa can be cited as the intermediate layer. As stated above, netiher of the Ni plated layers moderate thermal stress, and the solder layer 124 likewise does not perform this function.

Thus, Ishikawa fails to teach the first metal plate and the intermediate layer of claim 3. As a proper anticipation rejection requires that the cited reference teach each and every element of the claim, it is submitted that the present rejection of claim 3 lacks merit. Accordingly, reconsideration and withdrawal of the rejection of claim 3 is requested. Claims 5, 6, 11 – 14, and 16 depend from claim 3 and are likewise allowable over the cited art.

With further reference to claim 6, the semiconductor device of claim 3 recites that the intermediate layer for moderating thermal stress comprises a carbon-copper composite material. The Examiner listed claim 6 as being rejected based on Ishikawa, however failed to specify that Ishikawa teaches the feature recited by claim 6. Following a review of specification of Ishikawa, it is asserted that Ishikawa is silent as to this feature. Particularly, neither of the Ni plated layers (126, 128)

disposed between the upper electrode (116) and the IC chip (108) are taught as comprising a carbon-copper material. Further, the solder layer (124) of Ishikawa is not taught as comprising a carbon-copper material.

Thus, Ishikawa fails to teach this feature of claim 6. Accordingly, notwithstanding the patentability of claim 3, claim 6 is considered independently allowable over the art. Withdrawal of the rejection of claim 6 is requested.

With further reference to claim 11, the semiconductor device of claim 3 is recited wherein the thickness of the second metal plate and the third metal plate is greater than a thickness of the first metal plate. This feature mirrors that of allowable claim 8 (but for the dependence from claim 3). As the feature of claim 8 was not deemed to be taught or suggested by Ishikawa, claim 11 is likewise considered allowable over the art. Withdrawal of the rejection of claim 11 is requested.

Claims 1 – 3, 5 – 7, and 9 – 16 were rejected under 35 U.S.C. 103(a) as being unpatentable over U.S. Patent No. 4,497,875 to Arakawa et al. (hereinafter, "Arakawa") in view of Ishikawa. The rejections are traversed for the following reasons.

The invention defined in claim 1 is directed toward a semiconductor device. The device includes a semiconductor element and a first metal plate, where the first metal plate is bonded to one side of the semiconductor element. An intermediate layer formed of a carbon-copper composite material is bonded to a side of the first metal plate opposite to the side the semiconductor element is bonded. A second metal plate is bonded to the side of the intermediate layer opposite the side the first metal plate is bonded on. An insulating layer is bonded to a side of the second

metal plate that is remote from the side of the second metal plate where the intermediate layer is bonded. A third metal layer is bonded to the remote side of the insulating member. The second and third metal plates have substantially equal thicknesses. Further, the first, second, and third metal plates are made of the same material.

Additionally, claim 1 has been amended to recite the features of claim 2, and claim 2 has been cancelled. Claim 1 was further amended in a manner similar to claim 3, such that a coefficient of thermal expansion for both the semiconductor element and the heat sink were defined as being different from one another. The intermediate layer absorbs and moderates the thermal stress caused by the difference in coefficients of thermal expansion.

Arakawa teaches a semiconductor device having a semiconductor element (73) bonded to a metal plate (23). The metal plate (23) has a copper coating film (63) disposed on a top surface thereof, with the top surface being bonded to the semiconductor element (73) through a brazing layer (83). The bottom surface of the metal plate (23) is bonded to a top surface of an insulating plate (1) through a brazing layer (33). The bottom surface of the insulating plate (1) is bonded to a heat sink (5) through a brazing layer (4).

As was discussed in Amendment "B", Arakawa fails to teach metal plates. Rather, Arakawa teaches metal brazing layers. To remedy this shortcoming of Arakawa, the Examiner cites to Ishikawa for teaching metal plates. The Examiner summarily states that "it would have been obvious to one of ordinary skill in the art to use Ishikawa et al.'s metal plates to modify Arakawa et al.'s metal layers for the purpose of protecting semiconductors (sic) devices against a thermal breakdown".

(Office action mail date 06/09/2008, page 10, lines 1 – 3).

Contrary to the Examiner's position, the two references provide no teaching, suggestion, or motivation to support the proposed combination. Particularly, the metal layers of Arakawa that the Examiner interprets as corresponding to the first, second, and third metal plates of claim 1 are in fact a copper film coated on a metal plate and brazing layers, respectively. The brazing layers of Arakawa are provided for bonding purposes, and are not amenable to substitution with a metal plate. If a metal plate were substituted for the brazing layers, the device would be rendered, at a minimum, less operable. The same can be said of the copper layer coated on the metal plate, as a substitution of the coating for a metal plate (which would be disposed on another metal plate) would render the device inoperable. Thus, even if Ishikawa could be looked to for teaching metal plates, it is asserted that the combination of the references is improper.

Further, even if the references were combined, Ishikawa likewise fails to teach metal plates. The layers of Ishikawa cited to for teaching metal plates are: a Ni layer (126), the upper electrode (116), and the lower electrode (114). The Ni layer is a coating similar to the brazing layers taught by Arakawa, and thus does not teach or suggest a metal plate. Turning to the electrodes, it is submitted that the disclosure of an electrode does not suggest, to one skilled in the art, a metal plate. In drawing this conclusion, the Examiner is making an assumption unsupported by the Arakawa specification.

Further still, even if the brazing layers of Arakawa could properly be interpreted as teaching metal plates, the combined references would still fail to teach or suggest that "the first, second, and third metal plates are made of the same

material", as required by claim 1. The Examiner looks to the copper coating film 63 and the brazing layers 33, 4 as teaching the first, second and third metal plates of claim 1. Arakawa specifically discloses that the copper coating film (63) and the brazing layers (33, 40) are not made of the same material. Further, one skilled in the art of brazing would recognize that not all brazing layers are necessarily made of the same material. Rather, the material forming a brazing layer is chosen so as to be a material that will provide a desired bonding strength between different metals. Therefore, the brazing layers of Arakawa are not necessarily formed of the same material, and, in the absence of further definition, do not teach plates made of the same material. This shortcoming is not remedied by the Ishikawa patent, as the electrodes are not disclosed as being formed of Ni. Consequently, the combined references fail to teach or suggest first, second, and third metal plates made of the same material.

Additionally, the combined references fails to teach or suggest that the first metal plate is "bonded to one side of the semiconductor device" and also has "an intermediate layer bonded to one side ... remote from the semiconductor element", as required by claim 1. To simplify, claim 1 recites that the first metal plate is bonded to the semiconductor device on one side (hereinafter, a top side) and is bonded to the intermediate layer on the opposite side (hereinafter, a bottom side). Arakawa does not teach such a structure.

If brazing layers teach metal plates, as asserted by the Examiner, then Arakawa teaches a metal plate (brazing layer (83)) disposed between the first metal plate (copper coating film (63)) and the semiconductor element (73). Thus, contrary to the Examiner's assertion, the copper coating film (63) is bonded to a metal plate

(the brazing layer (83)), with the metal plate (brazing layer (83)) being bonded to the semiconductor element (73). Arakawa does not teach the first metal plate (copper coating film (63)) being bonded to the semiconductor element (73) itself. Ishikawa fails to teach the claimed structure for the reasons discussed above. Thus, the combined references fail to teach or suggest this additional feature of claim 1.

For these reasons, it is asserted that the combined references fail to teach or suggest all features of claim 1, and therefore do not render claim 1 obvious. Reconsideration and withdrawal of the rejection is requested. Claims 7 – 10 and 15 depend from claim 1 and are likewise considered allowable over the art.

With reference to claim 3, the arguments presented above in favor of the patentability of claim 1 are considered relevant, and are hereby incorporated by reference. Accordingly, claim 3 is considered allowable over the cited art. Claims 5, 6, 11 – 14, and 16 depend from claim 3 and are likewise considered allowable.

With further reference to claims 15 and 16, the devices recited in claims 1 and 3, respectively, further recite that the semiconductor element is directly bonded to the first side of the metal plate and the second side of the metal plate is directly bonded to the first side of the intermediate layer. The language in these claims is presented to preclude the Examiner's rationale that the semiconductor device (731) or Arakawa is "bonded by layers" to the copper film (63). There are other layers disposed between the semiconductor device (731) and the copper film (63) in the Arakawa disclosure. Accordingly, the two layers are not "directly bonded" to one another, as required by claims 15 and 16.

Accordingly, notwithstanding the patentability of claims 1 and 3, claims 15 and 16 are considered independently patentable. Reconsideration and withdrawal

of the rejections is requested.

In light of the foregoing, it is respectfully submitted that the present application is in a condition for allowance and notice to that effect is hereby requested. If it is determined that the application is not in a condition for allowance, the Examiner is invited to initiate a telephone interview with the undersigned attorney to expedite prosecution of the present application.

If there are any additional fees resulting from this communication, please charge same to our Deposit Account No. 18-0160, our Order No. SHM-16366.

Respectfully submitted,

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